This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (canceled)

Claim 2 (currently amended): An apparatus for processing a signal used to communicate a block of data representing at least one symbol, the apparatus comprising:

a Fourier transform circuit for performing at least one Fourier transform on ~~a~~ said signal ~~used to communicate a block of data representing at least one symbol~~;

a buffer coupled to said Fourier transform circuit for buffering data produced from an output of said Fourier transform circuit;

a jitter compensation filter coupled to said buffer for performing a filtering operation on data obtained from said buffer corresponding to said block of data to generate a filtered block of data, the jitter compensation filter having an update input for receiving a filter coefficient update signal;

an error calculation module coupled to the update input of the jitter compensation filter, the error ~~compensation~~ calculation module generating the filter coefficient update signal from at least one signal error estimate made from the filtered block of data output by the jitter compensation filter; and

a control circuit coupled to said error calculation module for determining as a function of said at least one signal error estimate, when to output said filtered block of data.

Claim 2 (previously presented): The apparatus of claim 1, further comprising:

a channel compensation circuit for receiving said block of data and performing a channel compensation operation on at least a portion of said block of data prior to the block of data being stored in said buffer for processing by said jitter compensation filter.

Claim 3 (original): The apparatus of claim 2, wherein said block of data represents a plurality of symbols, the apparatus further comprising:

demodulator circuitry coupled to an output of the jitter compensation filter.

Claim 4 (previously presented): The apparatus of claim 1, wherein the error calculation module includes:

means for generating a decision directed error value.

Claim 5 (currently amended): An apparatus for processing a signal used to communicate a block of data representing at least one symbol, the apparatus comprising:

a Fourier transform circuit for performing at least one Fourier transform on ~~a~~ said signal ~~used to communicate a block of data representing at least one symbol~~;

a buffer coupled to said Fourier transform circuit for buffering data produced from an output of said Fourier transform circuit;

a jitter compensation filter coupled to said buffer for performing a filtering operation on data obtained from said buffer corresponding to said block of data to generate a filtered block of data, the jitter compensation filter

having an update input for receiving a filter coefficient update signal; and

an error calculation module coupled to the update input of the jitter compensation filter, the error ~~compensation~~ calculation module generating the filter coefficient update signal from at least one signal error estimate made from the filtered block of data output by the jitter compensation filter, wherein the error calculation module includes:

means for generating a decision directed error value;

means for generating a pilot directed error value; and

a selection device for selecting one of the decision directed error value and the pilot directed error value to be output.

Claim 6 (currently amended): An apparatus for processing a signal used to communicate a block of data representing at least one symbol, the apparatus comprising:

a Fourier transform circuit for performing at least one Fourier transform on a said signal ~~used to communicate a block of data representing at least one symbol~~;

a buffer coupled to said Fourier transform circuit for buffering data produced from an output of said Fourier transform circuit;

a jitter compensation filter coupled to said buffer for performing a filtering operation on data obtained from said buffer corresponding to said block of data to generate a filtered block of data, the jitter compensation filter having an update input for receiving a filter coefficient update signal; and

an error calculation module coupled to the update input of the jitter compensation filter, the error ~~compensation~~ calculation module generating the filter coefficient update signal from at least one signal error estimate made from the filtered block of data output by the jitter compensation filter, wherein the error calculation module includes:

means for generating a decision directed error value;

means for generating a non-decision directed error value; and

a selection device for selecting one of the decision directed error value and the non-decision directed error value to be output.

Claim ~~8~~ 7 (previously presented): The apparatus of claim ~~7~~ 6, further comprising:

an input buffer coupled to the jitter compensation filter for storing said block of data while ~~it~~ being processed multiple times by said jitter compensation filter.

Claims 9 and 10 (canceled)

Claim ~~11~~ 8 (currently amended): An apparatus for processing a signal used to communicate a block of data representing at least one symbol, the apparatus comprising:

a Fourier transform circuit for performing at least one Fourier transform on ~~a~~ said signal ~~used to communicate a block of data representing at least one symbol~~;

a buffer coupled to said Fourier transform circuit for buffering data produced from an output of said Fourier transform circuit;

a jitter compensation filter coupled to said buffer for performing a filtering operation on data obtained from said buffer corresponding to said block of data to generate a filtered block of data, the jitter compensation filter having an update input for receiving a filter coefficient update signal, said buffer storing said block of data while said block of data is processed multiple times by said jitter compensation filter;

an error calculation module coupled to the update input of the jitter compensation filter, the error ~~compensation~~ calculation module generating the filter coefficient update signal from at least one signal error estimate made from the filtered block of data output by the jitter compensation filter; and

an output control device for determining when to output the filtered block of data generated by said jitter compensation filter.

Claim ~~12~~ 9 (original): The apparatus of claim ~~11~~ 8, wherein the output control device includes:

means for determining when said block of data has been filtered a fixed number of times by the jitter compensation filter.

Claim ~~13~~ 10 (original): The apparatus of claim ~~11~~ 8,

wherein the output control device includes an input for receiving the filter coefficient update signal generated by said error calculation module; and

wherein the jitter compensation filter further includes means for resetting filter coefficient values to a set of initial values in response to a reset signal generated by said output control device.

Claims 14 and 15 (canceled)

Claim ~~16~~ 11 (previously presented): A system for processing a multi-tone signal, the system including:

a Fourier transform circuit for performing at least one Fourier transform on said multi-tone signal;

a channel compensation module coupled to said Fourier transform circuit for performing a channel compensation operation on said multi-tone signal after processing by said Fourier transform circuit;

a buffer coupled to said Fourier transform circuit for buffering the channel compensated multi-tone signal;

a jitter compensation module coupled to said buffer for performing a jitter reduction operation on the buffered channel compensated multi-tone signal, wherein the jitter compensation module includes: a jitter compensation filter with programmable filter tap weights, and means for iteratively updating the filter tap weights as a function of the jitter compensation filter output; and

a control circuit for determining when the output of the jitter compensation filter should be used as the output of the jitter compensation module.

Claim ~~17~~ 12 (previously presented): The system of claim ~~16~~ 11, wherein the means for iteratively updating the filter tap weights includes:

a signal error estimation circuit for generating from the output of the jitter compensation filter a measure of a symbol error.

Claim 13 (previously presented): A system for processing a multi-tone signal, the system including:

a Fourier transform circuit for performing at least one Fourier transform on said multi-tone signal;

a channel compensation module coupled to said Fourier transform circuit for performing a channel compensation operation on said multi-tone signal after processing by said Fourier transform circuit;

a buffer coupled to said Fourier transform circuit for buffering the channel compensated multi-tone signal;

a jitter compensation module coupled to said buffer for performing a jitter reduction operation on the buffered channel compensated multi-tone signal, wherein the jitter compensation module includes : a jitter compensation filter with programmable filter tap weights, and means for iteratively updating the filter tap weights as a function of the jitter compensation filter output, wherein the means for iteratively updating the filter tap weights includes a signal error estimation circuit for generating from the output of the jitter compensation filter a measure of a symbol error; and

means for resetting the jitter compensation filter tap weights to an initial set of values in response to the control circuit determining that the output of the jitter compensation filter should be used as the output of the jitter compensation filter.

Claim ~~19~~ 14 (previously presented): A method of processing a multi-tone signal, the method comprising the steps of:

performing a Fourier transform operation on the multi-tone signal;

buffering a block of samples produced from the output of said Fourier transform operation; and

performing a jitter compensation operation, said jitter compensation operation including:

i) operating a filter having a plurality of tap weights to filter said block of samples to produce a filtered block of data;

ii) determining a signal error from the filtered block of data;

iii) updating at least one of said plurality of tap weights in said filter as a function of the determined signal error; and

iv) repeating steps i, ii, and iii until a filter updating stop criterion is satisfied.

Claim ~~20~~ 15 (original): The method of claim ~~19~~ 14, further comprising the step of:

supplying the filtered block of data output by said filter when said filter updating criterion is satisfied to subsequent receiver circuitry.

Claim ~~21~~ 16 (original): The method of claim ~~19~~ 14, wherein said filter updating stop criterion is the completion of a fixed number of filtering operations on said block of data.

Claim ~~22~~ 17 (original): The method of claim ~~21~~ 16, wherein said filter updating criterion is a failure in the signal error to exhibit an improvement over the previous signal error.

Claim ~~23~~ 18 (original): The method of claim ~~19~~ 14, wherein said step of determining a signal error includes generating a decision directed error value.

Claim ~~24~~ 19 (original): The method of claim ~~19~~ 14, wherein said step of determining a signal error includes generating a non-decision directed error value.

Claim ~~25~~ 20 (previously presented): The method of claim ~~19~~ 14, further comprising:

prior to performing said buffering, performing a channel compensation operation on said block of data.

Claim ~~26~~ 21 (original): The method of claim ~~25~~ 20, a single channel compensation operation is performed on the block of data in a first period of time; and

step i, ii and iii are performed multiple times in a time period which is equal to or shorter than the first time period.